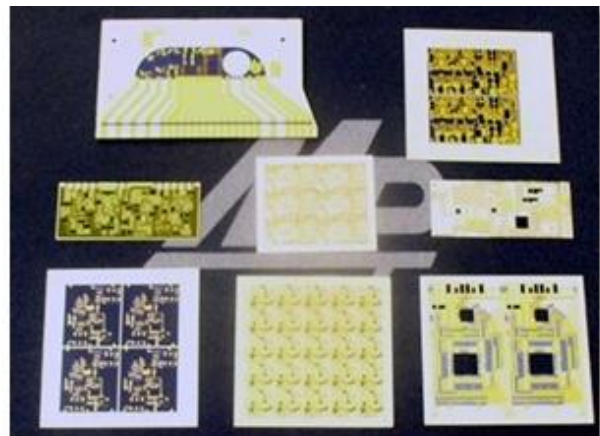




Micro-Precision Technologies (MPT) is an independent manufacturer of hybrid integrated circuits, multichip modules, and high-precision thick film substrates for the military, medical, avionics, optoelectronics, and communications industries. Founded in 1987, MPT is ITAR registered, ISO 9001 certified, QML-38534 listed, and MIL-PRF-38534 qualified for hybrid microcircuit performance.



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## Thick Film Circuit Fabrication (Print and Fire)

### Layers (Single-Layer, Multi-Layer, Double-Sided)

|                              |  |
|------------------------------|--|
| Conductors                   | Au, Pt, PtAu, PdAu, PtPdAu<br>Ag, PtAg, PdAg, PtPdAg |
| Plated-Through Vias/Holes    | Connection top to bottom circuitry or to ground      |
| Solid-Filled Vias/Holes      | Connection top to bottom circuitry or to ground      |
| Dielectrics                  | Protection for underlying circuitry                  |
| Thick Film Printed Resistors | Alternative to surface mount resistors               |
| Overglaze                    | Protection for underlying circuitry                  |

### Substrates

|   |                            |
|---|----------------------------|
| 91% Alumina (Al <sub>2</sub> O <sub>3</sub> ) | As Fired, Lapped, Polished |
| 92% Alumina                                   | As Fired, Lapped, Polished |
| 96% Alumina                                   | As Fired, Lapped, Polished |
| 99.6% Alumina                                 | As Fired, Lapped, Polished |
| Aluminum Nitride (AlN)                        | Lapped, Polished           |
| Beryllium Oxide (BeO)                         | As Fired, Lapped           |
| Ferrite                                       | Lapped, Polished           |

### Substrate Processing

|                 |                    |
|-----------------|--------------------|
| Laser Scribe    | Single/Array       |
| Laser Drill     | Vias/Holes         |
| Laser Machining | Per Specification  |
| Diamond Saw Cut | ± 0.002" Tolerance |

### Assembly

|                     |   |
|---------------------|---|
| Surface Mount (SMT) | Conductive or Non-Conductive Epoxy<br>Solder Reflow<br>Solder Lead/Pin Attachment |
|---------------------|---|

## Wire Bonding

|                |                     |
|----------------|---------------------|
| Gold Ball      | 0.001"–0.003" Wire  |
| Gold Wedge     | 0.0005"–0.003" Wire |
| Aluminum Wedge | 0.001"–0.003" Wire  |

## Product Testing/Measurement

|   |   |
|---|---|
| Physical Dimensions (Ceramic)           | Verify conforming to customer specification |
| Continuity/Netlist Connection Integrity | Resistor measurement value verification     |
| Metallization Adhesion                  | Leach resistance (verify adhesion)          |
| Trace Thickness and Width               | Verify conforming to customer specification |
| Wire Bond Qualification/Pull Testing    | Bond strength                               |
| Wire Bond Qualification/Shear Testing   | Bond strength                               |
| Burn-In                                 | Circuit stabilization                       |
| Performance                             | Design confirmation                         |
| Environmental                           | Endurance verification                      |
| Leak Testing                            | Verify hermetic seal                        |

## Engineering/Support/CAD

|                    |                            |
|--------------------|----------------------------|
| Circuit Design     | Layout from schematic      |
| Circuit Conversion | Convert from PCB (G10/FR4) |
| Artwork Generation | Circuit pattern definition |

## Advanced Processes

|                                       |  |
|---------------------------------------|--|
| Packaging, Potting, and Encapsulation | Ceramic, Glass Fiber Filled Plastic, Diallyl Phthalate |
| Ceramic Glass Sealing                 | Ceramic Packages                                       |
| Plated Up Thick Film Circuits         | High Current/High Power<br>Ni, Cu, Au                  |

## Thick Film Design Guidelines

### Substrates (Alumina, Aluminum Nitride, Beryllium Oxide)

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|                   |   |
|-------------------|---|
| Nominal Thickness | 10, 15, 25, 30, 40, 50, 60 mils ± 5 mils<br>Other thicknesses achieved by lapping |
|-------------------|---|

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### Conductors

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|   |                         |
|---|-------------------------|
| Line Width (min.)                         | 0.005"                  |
| Space Width (min.)                        | 0.005"                  |
| Thickness (typ.)                          | 8–12+ microns per layer |
| Pull back (from diced edges, min.)        | 0.004", 0.010", 0.004"  |
| Pull back (from scribed edge, min)        | 0.004", 0.010", 0.004"  |
| Pull back (from edge of dielectric, min.) | 0.004", 0.010", 0.004"  |
| Alignment (front to back)                 | 0.004"–0.008"           |

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### Resistors

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|   |  |
|---|--|
| Line Width (min)                          | 0.005"–0.010"                                |
| Space Width (min.)                        | 0.005"–0.010"                                |
| Minimum width relative to conductor width | 0.010" less, centered                        |
| Minimum Overlap With Conductor            | 0.003"                                       |
| Minimum Value                             | 1 Ω  |
| Maximum Value                             | 20 MΩ  |
| Multiple Resistors (on one side of chip)  | Yes, parameter defined                       |
| Typical Tolerance                         | 1%, 2%, 5%, 10%                              |
| Minimum Chip Size                         | 0.040" × 0.040" standard, smaller negotiable |
| Minimum Overlap                           | 0.003"                                       |

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### Vias (Plated-Through or Solid-Filled)

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|                               |  |
|-------------------------------|--|
| Diameter (min., max.)         | 0.005", 0.20"<br>Depending on substrate material and thickness |
| Minimum metal overlap of pads | 0.010"   |

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## Thick Film Design Rules

- A. Placement of any conductor, resistor, or dielectric: minimum of 0.005" from substrate border.
- B. Standard tolerance:  $\pm 0.002$ " or 10%, whichever is greater.
- C. Areas where a wire-bond crosses over a conductor should be glassed.
- D. For multilayer or crossover conductors, dielectric should overlap first conductor by 0.010".
- E. Vias for multilayer dielectric should be 0.015"×0.015" standard, but 0.010"×0.010" may be used.
- F. Via fill pads should be same size as dielectric vias.
- G. Conductors should not be under any printed resistor.
- H. Conductor overlap standard is 0.010".
- I. Minimum resistor sizes should be 0.030"×0.030". Smaller geometry size may be used upon departmental approvals.
- J. Resistor length should be no more than 3.5 times resistor width.
- K. Resistor overlap: 0.005" min., 0.010" typical.
- L. Three resistor passes are recommended. More than five require engineering approval.
- M. Resistors are designed 20% below nominal value.
- N. Resistors are to be on the top most layer of the substrate.
- O. Via pad size is a minimum of 0.010" annular to nominal hole.
- P. Minimum distance of hole edge to finished substrate edge is 0.025" or thickness of substrate, whichever is greater.
- Q. Minimum spacing between holes is 0.025" or thickness of substrate, whichever is greater.
- R. Non-plated via holes should not have metallization closer than 0.005" to the hole.
- S. Minimum wire-bonding pad size is 0.015"×0.015". 0.010" width may be used as long as the bond pad is in the same direction as the wire.
- T. Areas where a chip is to be mounted must have a minimum clearance of 0.005" on each side of the chip. Design should be done as worst case using the largest geometry of a given chip.
- U. Wire-bonding should not be done directly on via.
- V. Components should not cover other components (e.g., caps over resistors, ICs over resistors, etc.).
- W. Minimum conductor line width 0.005".
- X. Minimum conductor line spacing 0.005".
- Y. Screened stacks of dielectric glass over 35 microns high should be stepped down with a 0.010" step on all four sides of the stack at or before each 35-micron height.